AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (currently amended) A computer capable of playing real time applications comprising:

a processing circuit configured to operate in a first power state, a second power state, and a third power state, said processing circuit consuming less power in said second power state than in said first power state, and said processing circuit consuming less power in said third power state than in said second power state; and

a real time subsystem coupled to said processing circuit, said real time subsystem comprising a buffer, said buffer configured to store data and output said data to an output device for playing said real time applications thereby enabling said processing circuit to enter said third power state while said buffer is outputting said data.


2. (original) The computer of claim 1, wherein said first power state is a full power state, said second power state is a light sleep state, and said third power state is a deep sleep state, said light sleep state further comprising a first light sleep state and a second light sleep state, wherein said processing circuit consumes less power in said second light sleep state than in said first light sleep state, and wherein said buffer stores said data while said processing circuit is in said full power state or said first light sleep state.


3. (original) The computer of claim 2, wherein said full power state is state C0, said first light sleep state is state C1, said second light sleep state is state C2, and said deep sleep state is state C3.

4. (original) The computer of claim 1, wherein said real time application subsystem is a video subsystem or an audio subsystem.

5. (original) The computer of claim 1, wherein said buffer is a FIFO buffer.

6. (original) A real time subsystem comprising:

a buffer configured to store data for use in said real time subsystem enabling a processing circuit of a computer to enter a deep sleep state while said computer is running said real time subsystem.

7. (original) The real time subsystem of claim 6, wherein said real time subsystem is a video subsystem or audio subsystem.

8. (original) A method of conserving power in a computer while playing a real time application comprising the steps of:

reading a storage medium of data for use in said real time application;

processing said data in a processing circuit configured to operate in a first power state, a second power state, and a third power state, said processing circuit consuming less power in said second power state than in said first power state, and said processing circuit consuming less power in said third power state than in said second power state;

storing said data in a buffer;

outputting said data from said buffer to a real time application output device; and

placing said processing circuit in said third power state while said buffer is outputting said stored data.

9. (original) The method of claim 8, wherein said first power state is a full power state, said second power state is a light sleep state, and said third power state is a deep sleep state, said light sleep state further comprising a first light sleep state and a second deep light state, wherein said processing circuit consumes less power in said second light sleep state than in said first light sleep state, and wherein said ~~said~~ storing occurs when said processing circuit is in said full power state.

10. (original) The method of claim 9, wherein said full power state is state C0, said first light sleep state is state C1, said second light sleep state is state C2, and said deep sleep state is state C3.

11. (original) The method of claim 8, wherein said storing step is completed when said buffer reaches a predetermined full level data condition, and said processing circuit is woken up from said third power state when said buffer reaches a predetermined low level data condition.

12. (original) The method of claim 11, wherein said first power state is a full power state, said second power state is a light sleep state, and said third power state is a deep sleep state, said light sleep state further comprising a first deep light state and a second light sleep state, wherein said processing circuit consumes less power in said second light sleep state than in

said first light sleep state, and when said processing circuit is said woken up, said processing circuit enters into said full power state.

13. (original) The method of claim 12, wherein said full power state is state C0, said first light sleep state is state C1, said second light sleep state is state C2, and said deep sleep state is state C3.

14. (original) A method of conserving power in a computer where at least one device has direct access to system memory comprising the steps of:

flushing cache memory of a processing circuit to said system memory of said computer, wherein said processing circuit is configured to operate in a first power state, a second power state, and a third power state, said processing circuit consuming less power in said second power state than in said first power state, and said processing circuit consuming less power in said third power state than in said second power state;

placing said processing circuit in said third power state; and

maintaining a first device power state in said at least one device, wherein said at least one device is configured to operate in said first device power state, a second device power state, and a third device power state, said device consuming less power in said second device power state than in said first device power state, and said device consuming less power in said third device power state than in said second device power state.

15. (original) The method of claim 14, wherein said first power state is a full power state, said second power state is a light sleep state, and said third power state is a deep sleep state, said light sleep state further comprising a first light sleep state and a second light sleep state,

wherein said processing circuit consumes less power in said second light sleep state than in said first light sleep state.

16. (original) The method of claim 15, wherein said full power state is state C0, said first light sleep state is state C1, said second light sleep state is state C2, and said deep sleep state is state C3.

17. (original) The method of claim 14, wherein said first device power state is a full device power state, said second device power state is a light sleep device state, and said third device power state is a deep sleep device state, said light sleep device state further comprising a first device light sleep state and a second device light sleep state, wherein said device consumes less power in said second device light sleep state than in said first device light sleep state.

18. (original) The method of claim 17, wherein said full device power state is state D0, said first device light sleep state is state D1, said second device light sleep state is state D2, and said deep sleep device state is state D3.

19. (withdrawn) A computer for improving security of system memory access when at least one device has direct access to system memory comprising:
a processing circuit configured to operate in a first power state, a second power state, and a third power state, said processing circuit consuming less power in said second power state than in said first power state, and said processing circuit consuming less power in said third power state than in said second power state; and

a bridge coupled to said system memory and said at least one device, said bridge having programmable control registers, said programmable control registers programmed to limit access of said at least one device to said system memory when said processing circuit is in said third power state.

20. (withdrawn) The computer of claim 19, wherein said programmable control registers can not be accessed by said at least one device having direct access to said system memory.

21. (withdrawn) The computer of claim 19, wherein said first power state is a full power state, said second power state is a light sleep state, and said third power state is a deep sleep state, said light sleep state further comprising a first light sleep state and a second light sleep state, wherein said processing circuit consumes less power in said second light sleep state than in said first light sleep state.

22. (withdrawn) The computer of claim 21, wherein said full power state is state C0, said first light sleep state is state C1, said second light sleep state is state C2, and said deep sleep state is state C3.

23. (withdrawn) The computer of claim 19, wherein said at least one device is an audio subsystem or video subsystem and said bridge is a host bridge or system bridge.

24. (withdrawn) A computer comprising:

a system clock control circuit configured to provide a plurality of clock signals; and

a plurality of devices configured to receive an associated one of said plurality of clock signals, wherein at least one of said devices has a full power device state, a light sleep power device state, and a deep sleep power device state, said at least one device consuming less power in said light sleep device state than in said full power device state, and said at least one device consuming less power in said deep sleep device state than in said light sleep device state, wherein said system clock control circuit independently controls each of said plurality of clock signals.

25. (withdrawn) The computer of claim 24, wherein each of said plurality of devices may be in said full power device state, said first light sleep device state, said second light sleep device state, or said deep sleep device state, and wherein each of said plurality of devices is responsive to each of said associated clock signals from said clock control circuit enabling each of said plurality of components to be in either said full power device state, said light sleep power device state, or said deep sleep power state independent of a power state of any other of said plurality of devices.

26. (withdrawn) The computer of claim 24, wherein one of said plurality of devices is responsive to an associated clock signal and is in said full power device state, while a remainder of said plurality of devices is in said deep sleep state.

27. (withdrawn) The computer of claim 24, further comprising:
a bus having a full power bus state, a light sleep power bus state, and a deep sleep power bus state, said bus consuming less power in said light sleep power bus state than in said full power bus state, and said bus consuming less power in said deep sleep bus state than in said

light sleep bus state, wherein each of said plurality of devices is coupled to said bus and wherein said at least one device is responsive to said associated clock signal to be in said full power device state, while said bus is in said deep sleep bus state.

28. (withdrawn) The computer of claim 27, wherein said bus is a PCI bus and said at least one device is an audio subsystem or video subsystem.

29. (withdrawn) A method of independently controlling power consumption of a plurality of devices in a computer comprising:

providing a plurality of independent clock signals to said associated plurality of devices, wherein each of said plurality of devices has a full power device state, a light sleep power device state, and a deep sleep power device state, each of said plurality of devices consuming less power in said light sleep device state than in said full power device state, and each of said plurality of devices consuming less power in said deep sleep device state than in said light sleep device state; and

providing an associated independent clock signal to at least one of said devices keeping said device in said full power state while a remainder of said plurality of devices may be in said full power device state, said light sleep device state, or said deep sleep device state.

30. (withdrawn) The method of claim 29, wherein said at least one device is an audio subsystem or a video subsystem.

31. (withdrawn) The method of claim 29, wherein said remainder of said plurality of devices is in said deep sleep state.

32. (withdrawn) The method of claim 29, wherein said plurality of devices are coupled to a bus, said bus having a full power bus state, a light sleep power bus state, and a deep sleep power bus state, said bus consuming less power in said light sleep power bus state than in said full power bus state, and said bus consuming less power in said deep sleep bus state than in said light sleep bus state, wherein said bus is in said deep sleep bus state while said at least one device coupled to said bus in said full power device state.

33. (withdrawn) The method of claim 32, wherein said bus is a PCI bus.

34. (currently amended) A computer capable of playing real time applications comprising:

a processing circuit;

an output device coupled to said processing circuit via a bus; and

a real time subsystem coupled to said processing circuit via said bus, said real time subsystem comprising a buffer, said buffer configured to store data and output said data to said output device for playing said real time applications thereby enabling said processing circuit to enter a deep sleep state while said buffer is outputting said data.